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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/476,862	01/03/2000	AKIRA TSUKIHASHI	005586-20026	8395

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HOGAN & HARTSON L.L.P.
500 S. GRAND AVENUE
SUITE 1900
LOS ANGELES, CA 90071-2611

EXAMINER	
PATEL, GAUTAM	
ART UNIT	**PAPER NUMBER**
2655	17

DATE MAILED: 04/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.	Applicant(s)
09/476,862	Tsukihashi
Examiner	**Art Unit**
Gautam R. Patel	2655

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Oct 15, 2002* .

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *3-12* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *3-12* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Response to Amendment

1. This is in response to amendment filed on 10-15-03 (Paper # 16).

2. Claims 3-12 remain for examination.

Claim Rejections - 35 U.S.C. § 103

3. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

4. Claims 3-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shinada et al., US. patent 5,436,875 (hereafter Shinada) in view of Landry et al., US. patent 5,434,997 (hereafter Landry).

As to claim 3, Shinada discloses the invention as claimed [see Figs. 1-16] including a buffer memory, a data processing circuit and a system control circuit, a write circuit comprising:

As to claim 3, Shinada discloses::

a. a buffer memory fig. 1, units 18 and 22] for temporarily storing the received data [col. 6, lines 1-5];

b. a data processing circuit [fig. 1, units 14 and 6] for preparing the recording data to record onto the disk [col. 3, line 61 to col. 4, line 2], based on the received data read from the buffer memory [col. 6, lines 54-59; and

c. a system control circuit [fig. 1, unit 10] for controlling writing and reading of the received data with respect to the buffer memory, and operation of the data processing circuit [col. 5, lines 40-42 and col. 5, lines 65-68], and

d. A writing circuit [fig.1, unit 4] for writing the recorded data supplied from the data processing circuit onto the disk [col. 5, lines 18-39];

e. wherein the system control circuit [fig. 1, unit 10] suspends operation of the data processing circuit until an amount of received data equivalent to a predetermined writing capacity [memory 22 drops below the fixed volume or not; col. 8, lines 34-35] has been stored in the buffer memory, and releases suspension of the operation of the data processing circuit when an amount of received data equivalent to the predetermined writing capacity has been stored in the buffer memory [col. 8, lines 19-55];

f. wherein the system control circuit stores an address successive to an address of received data last recorded [position information] onto the disk [data previously stored], as a recording start address on the disk, and controls the writing circuit so as to write the recording data supplied from the data processing circuit onto the disk as the recording start address [col. 1, lines 51-57; col. 5, lines 51-64 and col. 12, lines 48-68]; and

g. wherein the system control circuit synchronizes the recording data to be newly recorded onto the disk, supplied from the data processing circuit to the writing circuit, with recording data recorded on the disk [col. 6, lines 12-28], said data processing circuit being operated in synchronism with a reproduction clock obtained by reproducing the data already recorded on the disk [col. 2, lines 14-17; col. 7, lines 38-52; col. 9, lines 15-29].

Shinada discloses all of the above elements including system control circuit for suspending the operation of the data processing circuit [col. 8, lines 19-30]. Shinada

does not specifically disclose how his system is suspending this operation and details of the suspension circuit and data being placed in a suspended state by interrupting the power supply or by halting an operation clock to the extent claimed. However Landry clearly discloses:

the data processing circuit for recording data being placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock [col. 2, lines 19-40 and col. 16, lines 13-61; Landry]. Both Shinada and Landry are interested in controlling the recording operation of the data and avoiding wrong data recording by checking the data content against some reference point [such as threshold or fixed volume of data] and controlling the recording operation. Also both are aware that most of the data processing systems are interrupt driven and need to store data in the buffer because of interrupts that inherently arises from time to time. It would have been obvious to one of ordinary skill in the at the time of invention to have provided the system of Shinada with details of controlling the data recording by halting the system clock as disclosed by Landry, because doing so would have provided a mechanism for localizing an error or fault on the spot and easily correct it [see col. 1, lines 13-30; Landry], in order to implement the suggested invention of Shinada.
NOTE: Shinada clearly discloses that his invention can be practiced on ROM [non-erasable, write-once], RAM [read and write] or hybrid [some areas are ROM and some areas are RAM] [see col. 3, line 61 to col. 4, line 2].

5. As to claim 4, Shinada discloses:

. a motor control circuit [fig. 1, unit 7] for controlling a motor for driving the disk, wherein the motor control circuit controls the motor such that the disk rotates, while operation of the data processing circuit is suspended at a same speed as that at which the disk rotated immediately before the suspension of data recording [col. 5, lines 3-30 and col. 6, lines 35-40];
NOTE: Shinada discloses that disc rotates under constant linear velocity [col. 5, lines 5-6]. Shinada also discloses that disc is able to start the recording function again without

stopping the inputting the data signal S1. In other words the disc speed is constant before and after the suspension of the recording.

6. As to claim 5 Shinada does not specifically discloses that the buffer memory is set at a full memory capacity. "Official Notice" is taken that both the concept and the advantages of setting the buffer memory capacity at full capacity are well known in the art. It would have been obvious to provide a full capacity to buffer memory in Shinada's system as this setting the capacity to full allows the system to use the full capability of the buffer. Since real estate in the integrated circuits and on the board are at premium one of ordinary skill in the art would have been able to provide the mechanism to use full capability of the buffer so as not to waste premium space in the buffer. These concepts are well known in the art and do not constitute a patentably distinct limitation, per se [M.P.E.P. 2144.03].

7. As to claim 6, Shinada discloses:

the writing capacity of the buffer memory is set at the capacity of the buffer memory deducted by an amount of data expected to be written into the buffer memory before data recording onto the disk is resumed [col. 6, lines 16-27].

Shinada discloses all of the above elements. Shinada does not specifically discloses that the buffer memory is set at a full memory capacity. "Official Notice" is taken that both the concept and the advantages of setting the buffer memory capacity at full capacity are well known in the art. It would have been obvious to provide a full capacity to buffer memory in Shinada's system as this setting the capacity to full allows the system to use the full capability of the buffer. Since real estate in the integrated circuits and on the board are at premium one of ordinary skill in the art would have been able to provide the mechanism to use full capability of the buffer so as not to waste premium space in the buffer. These concepts are well known in the art and do not constitute a patentably distinct limitation, per se [M.P.E.P. 2144.03].

NOTE: recording or writing stops when the memory capacity minus expected data limit is reached. In other words memory 18 data falls below a prescribed value or threshold.

8. As to claim 7, Shinada discloses:

a.a buffer memory fig. 1, units 18 and 22] for temporarily storing the received data [col. 6, lines 1-5];

b.a data processing circuit [fig. 1, units 14 and 6] for preparing the recording data to record onto the disk, based on the received data read from the buffer memory [col. 6, lines 54-59; and

c.a system control circuit [fig. 1, unit 10] for controlling writing and reading of the received data with respect to the buffer memory, and operation of the data processing circuit [col. 5, lines 40-42 and col. 5, lines 65-68]; and

d.a writing circuit [fig. 1, unit 4] for writing the recorded data supplied from the data processing circuit, onto the disk, wherein the system control circuit suspends operation of the data processing circuit until an amount of received data equivalent to a predetermined writing capacity has been stored in the buffer memory, and releases suspension of the operation of the data processing circuit to resume writing of the recording data onto the disk by the writing circuit when an amount of received data equivalent to the predetermined writing capacity has been stored in the buffer memory [col. 8, lines 19-55].

Shinada discloses all of the above elements including system control circuit for suspending the operation of the data processing circuit [col. 8, lines 19-30]. Shinada does not specifically disclose how his system is suspending this operation and details of the suspension circuit and data being placed in a suspended state by interrupting the power supply or by halting an operation clock to the extent claimed. However Landry clearly discloses:

the data processing circuit for recording data being placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock [col. 2, lines 19-40 and col. 16, lines 13-61; Landry]. Both Shinada and Landry are interested in

controlling the recording operation of the data and avoiding wrong data recording by checking the data content against some reference point [such as threshold or fixed volume of data] and controlling the recording operation. Also both are aware the most of the data processing system are interrupt driven and need to store data in the buffer because of interrupts. It would have been obvious to one of ordinary skill in the at the time of invention to have provided the system of Shinada with details of controlling the data recording by halting the system clock as disclosed by Landry, because doing so would have provided a mechanism for localizing an error or fault on the spot and easily correct it [see col. 1, lines 13-30; Landry], in order to implement the suggested invention of Shinada.

9. As to claim 8, Shinada discloses:

the system control circuit stores an address successive to an address of received data last recorded [position information] onto the disk [data previously stored], as a recording start address on the disk, and controls the writing circuit so as to write the recording data supplied from the data processing circuit onto the disk as the recording start address [col. 1, lines 51-57; col. 5, lines 51-64 and col. 12, lines 48-68].

10. As to claim 9, Shinada discloses:

wherein the system control circuit synchronizes the recording data to be newly recorded onto the disk, supplied from the data processing circuit to the writing circuit, with recording data recorded on the disk , said data processing circuit being operated in synchronism [simultaneously] with a reproduction clock obtained by reproducing the data already recorded on the disk [col. 2, lines 14-17; col. 7, lines 38-52; col. 9, lines 15-29].

11. As to claim 10, Shinada discloses:

a motor control circuit [fig. 1, unit 7] for controlling a motor for driving the disk, wherein the motor control circuit controls the motor such that the disk rotates, while

operation of the data processing circuit is suspended at a same speed as that at which the disk rotated immediately before the suspension of data recording [col. 5, lines 3-30 and col. 6, lines 35-40];
NOTE: Shinada discloses that disc rotates under constant linear velocity [col. 5, lines 5-6]. Shinada also discloses that disc is able to start the recording function again without stopping the inputting the data signal S1. In other words the disc speed is constant before and after the suspension of the recording.

12. As to claim 11 Shinada does not specifically discloses that the buffer memory is set at a full memory capacity. "Official Notice" is taken that both the concept and the advantages of setting the buffer memory capacity at full capacity are well known in the art. It would have been obvious to provide a full capacity to buffer memory in Shinada's system as this setting the capacity to full allows the system to use the full capability of the buffer. Since real estate in the integrated circuits and on the board are at premium one of ordinary skill in the art would have been able to provide the mechanism to use full capability of the buffer so as not to waste premium space in the buffer. These concepts are well known in the art and do not constitute a patentably distinct limitation, per se [M.P.E.P. 2144.03].

13. As to claim 12, Shinada discloses:

the writing capacity of the buffer memory is set at full memory capacity of the buffer memory deducted by an amount of data expected to be written into the buffer memory before data recording onto the disk is resumed [col. 6, lines 16-27].
NOTE: recording or writing stops when full memory capacity minus expected data limit is reached. In other words memory 18 data falls below a prescribed value or threshold.

Shinada and Landry were cited as prior art references in paper no. 15, mailed 8-6-02.

14. Applicant's arguments filed on 10-15-03 (Paper # 16) have been fully considered but they are not deemed to be persuasive for the following reasons.

15. In the REMARKS, the Applicant argues as follows:

A) That: "It is not a feature of the present invention to simply interrupt the operation when there is no data.

The cited reference do not discloses or suggest such a configuration in accordance with the present invention." [page 3, para. 3-4; REMARKS].

FIRST: It would be useless to interrupt operation when there is no data. Also without data there is no operation on data, and without operation there is no interruption at all.

SECOND: If there is something different the Applicants are trying to claim, than that aspect is not being claimed.

THIRD: As to operation of interruption, when needed is very clearly disclosed by Shinada [see rejection of claim 3 supra].

B) That: "The present invention involves a write-once disk in which recorded data cannot be erased. Accordingly, a configuration is achieved in which the recorded data is read out and new data is written successively, starting at the address of the last recorded data. In, Shinada, where rewriting on the disk can be performed, such reference does not show or suggest the configuration of the present invention." [page 3, para. 6 to page 4, para. 1; REMARKS].

Nothing can be further from the truth. Shinada clearly discloses that his invention can be practiced on ROM [write-once], or RAM or even hybrid disk. See rejection of claim 3 supra.

C) That: "Although Shinada describes that data recording is performed intermittently in a manner such that data discontinuity can be avoided, there is no

detailed description of how data is recorded after resumption of recording." [page 4, para. 3; REMARKS].

FIRST: Shinada is not required to disclose any detail.

SECOND: If there are more details of recording according to present invention, they are NOT claimed. The Examiner is simply trying to address what is being claimed, and not what the Applicants might have.

D) That: "In the present invention, on the other hand, data already stored in the disk is read, and data is additionally written on the disk in synchronism with the read data. In this manner, additional data write is enabled without generation gaps, even on a write-once disk such as CD-R. Such a configuration is not disclosed or suggested by Shinada.

FIRST: Such a configuration is clearly disclosed [see claim 3, supra].

SECOND: Inherently you have start writing from the place from where the writing has stopped in any good system, so as to save space. This is done by marking the address from where interrupt has occurred. Shinada clearly discloses all these aspects.

E) That: "it appears that Shinada contains no description concerning additional writing as claimed in the present invention, and as described above." [page 5, para. 1; REMARKS].

Additional data write to the extent claimed is exactly done by the Shinada. After data write stops from some interrupt, additional data write is taking place.

F) That: "as previously noted ....the object of reproducing" [page 5, para. 2; REMARKS].

This argument was answered in previous action paper no. 15, dated 8-6-02; section A).

G) That: "In claim 3, for example, such claim has been amended to define a recording data processing circuit ...recording data "onto a non-erasable, write-once disk" [original quote]." [page 5, para. 4; REMARKS].

See section A), supra.

16. **THIS ACTION IS MADE FINAL**. See M.P.E.P. § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact information

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gautam R. Patel whose telephone number is (703) 308-7940. The examiner can normally be reached on Monday through Thursday from 7:30 to 6.

The appropriate fax number for the organization (Group 2650) where this application or proceeding is assigned is (703) 872-9314.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ms. Doris To can be reached on (703) 305-4827.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 305-4700 or the group Customer Service section whose telephone number is (703) 306-0377.

Gautam R. Patel
Patent Examiner
Group Art Unit 2655

March 31, 2003

DORIS H. TO 4/4/03
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600